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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
LE, THONG QUOC

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/050,342	Applicant(s) PAN ET AL.	
	Examiner Thong Q. Le	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,8-11 and 16-22 is/are rejected.

7)☒ Claim(s) 2-7 and 12-15 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-22 are presented for examination.

Information Disclosure Statement

1. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on January 16, 2002.

2. Information disclosed and list on PTO 1449 was considered.

Specification

3. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

4. The drawings are objected to under 37 CFR 1.83(a) because they fail to show gate 270-273 (page 12, line 7), switch 134a (page 12, line 11) as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1,8-11,16-22** are rejected under 35 U.S.C. 102(b) as being anticipated by Van Buskirk et al. (U.S. Patent No. 5,282,170)

Regarding claims 1 and 11, Van Buskirk et al. disclose a method of erasing a core memory cell using a negative gate voltage in a semiconductor memory device (Column 1, lines 6-14), comprising:

generating an erase signal to begin an erase operation (Figure 1, 58);

generating a pre-charge signal according to the erase signal (Figure 7, 702);

pre-charging negative pump MOS regulation capacitors (Figure 1, 16) according to the pre-charge signal;

regulating a negative pump voltage (Figure 1, 12) using the pre-charged negative pump MOS regulation capacitors; and

erasing the core memory cell by applying a negative gate voltage (Figure 1, 38) to the core memory cell using the regulated negative pump voltage.

Regarding claims 8 and 16, Van Buskirk et al. disclose wherein pre-charging the negative pump MOS regulation capacitors comprises connecting a reference voltage (Figure 1, VREF) to the capacitors according to the pre-charge signal.

Regarding claims 9 and 21, Van Buskirk et al. disclose wherein pre-charging the negative pump MOS regulation capacitors comprises connecting the reference voltage to the capacitors for about 160ns (Figure 2, Column 4, lines 42-45).

Regarding claims 10 and 18, Van buskirk et al. disclose wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance (Figure 1, C1) with a first terminal connected to a ground (Figure 1) and a second terminal connected to a switch (Figure 1, switch transistor connected with C1 at node 108) , and a second capacitance (Figure 1, C2) with a first terminal connected to the switch (Figure 1, switch transistor connected with C2 at node 108) and a second terminal connected to a negative voltage pump (Figure 1, C2 connected with NEGPUMP at node 42) , and wherein pre-charging the negative pump MOS regulation capacitors connecting a reference voltage (Figure 1, VREF) to the second terminal of the first capacitance and the first terminal of the second capacitance using the switch.

Regarding claim 19, Van Buskirk et al. disclose an apparatus for pre-charging negative pump MOS regulation capacitors (Figure 1, 16, Figure 7) during a core cell erase operation (Column 11, lines 42-44) in a memory device (ABSTRACT), comprising:

a switch (Figure 1, transistor between 108 and VREF, Figure 7, 3/16) connected between a reference voltage (Figure 7, VREF) and the negative pump MOS regulation capacitors (Figure 1, C1, C2) ; and

a pre-charge control circuit (Figure 7, N101, N102, Column 11, lines 31-32) providing a pre-charge signal (Figure 7, PGMRB) to the switch ;

wherein the switch is operative to selectively connect the reference voltage to the negative pump MOS regulation capacitors according to the pre-charge signal (Column 11, lines 35-42).

Regarding claim 20, Van Buskirk et al. disclose wherein the pre-charge control circuit receives an erase signal (Figure 7, ERB) during the core cell erase operation , and generates the pre-charge signal for a time period, and wherein the switch connects the reference voltage to the negative pump MOS regulation capacitors during the time period (Column 11, lines 35-45).

Regarding claim 21, Van Buskirk et al. disclose wherein the time period is about 160ns (Figure 2, Column 4, lines 42-45).

Regarding claim 22, Van Buskirk et al. disclose wherein the negative pump MOS regulation capacitors comprise a capacitive voltage divider circuit having a first capacitance (Figure 1, C1) with a first terminal connected to a ground (Figure 1, C1 coupled to Ground) and a second terminal connected to the switch (Figure 1, C1 coupled at 108, switch transistor), and a second capacitance (Figure 1, C2) with a first terminal connected to the switch (Figure1, C2 connected at 108 of switch transistor) and a second terminal connected to a negative voltage pump (Figure1) , and wherein the switch is operative to selectively pre-charge the negative pump MOS regulation capacitors by connecting the reference voltage to the second terminal of the first

capacitance and the first terminal of the second capacitance according to the pre-charge signal (Column 4, lines 49-68, Column 5, lines 1-9).

Allowable Subject Matter

7. **Claims 2-7, 12-15** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-7, 12-15 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Van Buskirk et al. (U.S. Patent No. 5,282,170), and others, does not teach the claimed invention having a method of erasing a core memory having a pre-charge signal Figure 4, 132 having a pulse duration in Figure 8, 260, ONESHOT.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 703-306-9123. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Thong Q. Le
Examiner
Art Unit 2818

April 27, 2002